# Silicon-Germanium Devices for CMOS Formed by Ion Implantation and Solid Phase Epitaxial Regrowth

## Field of the Invention

The present invention relates to methods and apparatus for the manufacture of silicon-germanium semiconductor devices.

## Background of the Invention

Complementary metal-oxide-semiconductor (CMOS) technology is widely used in integrated circuits (ICs) due to the lower power consumption of CMOS ICs, as compared to previously preferred NMOS ICs. CMOS is so named because it uses both p- and n-channel transistors in its ICs. However, one of the most fundamental and serious limitations of CMOS technology resides in the p-channel device. Generic, one-micron processes reflect such limitations in the disparate field-effect mobilities associated with n-channel and p-channel devices within a CMOS IC. In such devices, p-channel field-effect hole mobility is approximately two to three times lower than n-channel field-effect electron mobility. Thus, in order to achieve optimum symmetrical switching and driving capabilities, p-channel devices must be more than twice as large as n-channel devices, which undesirably affects packing density of an IC.

To overcome device-operational limitations in bipolar technology, as used in amplifying and switching devices, silicon-germanium ($Si_{1-x}Ge_x$)/Si heterojunctions were developed. $Si_{1-x}Ge_x$ has an associated band gap that is smaller than that of the silicon. When such a material is used for the emitter material in a bipolar transistor, a higher emitter-injection efficiency is obtained due to the bandgap difference between the silicon base material and the emitter material. To form a $Si_{1-x}Ge_x$/Si

heterojunction, molecular beam epitaxy (MBE) and ultrahigh-vacuum chemical vapor deposition (UHV CVD) are currently used.

It is desirable to adapt $Si_{1-x}Ge_x$/ Si heterojunction technology to improving field-effect mobilities of p-channel MOS devices used in CMOS ICs. However, while MBE and UHV CVD are two methods for forming a $Si_{1-x}Ge_x$/Si heterojunction, both techniques are not compatible with large-scale manufacturing processes, such as commonly used to form CMOS ICs. MBE and UHV CVD are complicated and expensive. MBE and UHV CVD were developed for use in fabricating bipolar devices, which are intolerable towards microdefects and dislocations resulting from strained layers, due to their extremely small base widths, which require very sharp profiles and transitions. It was not critical to develop an efficient, high volume technique for the fabrication of $Si_{1-x}Ge_x$ layers. Thus, it has not been possible to adapt $Si_{1-x}Ge_x$/Si heterojunction technology to the large volume manufacture of CMOS ICs. MOS devices are much more tolerant of microdefects and dislocations, since there is no concern about emitter-collector shorts resulting from the extremely small base widths inherent in bipolar devices.

Furthermore, conventional silicon CMOS transistor gates are formed by thermally oxidizing the silicon substrate. When a $Si_{1-x}Ge_x$ layer is formed on a silicon substrate, by MBE or UHV CVD, stable gate oxides can not be later formed on the $Si_{1-x}Ge_x$ layer. Oxides of Ge are not stable, thus, other ways of forming a gate oxide layer are being investigated. One way of forming a stable gate oxide over a $Si_{1-x}Ge_x$ layer is by depositing low temperature CVD oxides. However, such oxides have a resulting undesirable higher surface state density. Another way of forming a stable gate oxide over a $Si_{1-x}Ge_x$ layer is by reoxidation of a silicon cap layer applied over the $Si_{1-x}Ge_x$ layer. However, using a silicon cap layer results in a buried channel structure with an undesirably large effective gate oxide thickness. Furthermore, at high gate voltages, many of the $Si_{1-x}Ge_x$ layer carriers migrate to the silicon cap layer. The net result is a loss in device performance.

There is a need for a method of large volume manufacturing of Si-Ge semiconductor devices. In particular, there is a need for a method of large volume manufacturing of silicon-germanium CMOS ICs, in which a stable gate oxide layer can exist over a $Si_{1-x}Ge_x$ transistor channel.

## Summary of the Invention

The present invention teaches a method and apparatus for large volume manufacturing of Si-Ge complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs). $Si_{1-x}Ge_x$ is formed under existing gate oxide layers, eliminating the problem of forming stable gate oxides directly over a $Si_{1-x}Ge_x$ layer. A high dose Ge layer is implanted under the gate oxide layer. Next, a $Si_{1-x}Ge_x$ layer is grown by solid phase epitaxial (SPE) regrowth, such that lattice mismatch is minimized between the $Si_{1-x}Ge_x$ layer and the underlying Si substrate. SPE is performed in a low temperature furnace, for approximately ten minutes. Implantation and anneal steps are commonplace in the large volume manufacture of CMOS ICs. Thus, this invention does not add significant cost or complexity to the manufacture of CMOS ICs, while providing the ability to manufacture high volume CMOS ICs with enhanced field effect hole mobility.

According to one aspect of the invention, the $Si_{1-x}Ge_x$ layer formed in this invention has a critical layer thickness, which depends on the molar fraction, x, of germanium present in the $Si_{1-x}Ge_x$ compound formed. As long as the critical layer thickness is not exceeded, $Si_{1-x}Ge_x$ will form defect-free during SPE regrowth. By forming p-channels in accordance with the method of the invention, valuable chip space is conserved, enabling high density chips to be formed. P-channel transistors are able to be formed in approximately the same amount of space as n-channel transistors due to the increased field effect hole mobility, while obtaining symmetrical switching and driving capabilities.

## Brief Description of the Drawings

Figures 1A to 1C are cross-sectional representations of the method of forming Si-Ge CMOS ICs.

Figure 2 is a graphical representation of the critical thickness of a $Si_{1-x}Ge_x$ layer with respect to the molar fraction of germanium, x, present in the layer.

## Description of the Embodiments

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims. Numbering in the Figures is usually done with the hundreds and thousands digits corresponding to the figure number, with the exception that the same components may appear in multiple figures.

In the manufacture of p-channel metal-oxide-semiconductor (PMOS), transistors for complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) are formed, having $Si_{1-x}Ge_x$/Si heterojunctions. A $Si_{1-x}Ge_x$/Si heterojunction is formed between the substrate and the channel region. The presence of the heterojunction in each PMOS transistor substantially increases the speed of such devices due to an increase in the field-effect hole mobility. By increasing the speed of PMOS devices, they can be made smaller. Thus, chip density is improved.

The first steps in the manufacture of a PMOS transistor in accordance with the method of the invention are those used in the conventional manufacture of PMOS transistors, as shown in Figure 1A. These steps are: formation of active device

areas on a silicon substrate 110, defined by field oxide 112 and growth of a gate oxide layer 114 on the silicon substrate 110, as well known to one skilled in the art. The silicon substrate 112 is either a (n-) substrate or it comprises an (n-) well formed in a (p-) substrate.

Next, a $Si_{1-x}Ge_x$ channel is formed under the existing gate oxide layer 114, shown in Figure 1A, eliminating the problem of forming stable gate oxides directly over a $Si_{1-x}Ge_x$ layer. Using conventional photoresist masking and patterning techniques, all but the gate oxide layer 114 are protected from implantation with a photoresist layer 115. Then, a high dose (approximately $2 \times 10^{16}$ atoms/cm$^2$) of Ge is implanted under the gate oxide layer 114. The Ge is implanted to a depth of between 100 to 1,000 angstroms, preferably approximately 300 angstroms, to form an implanted region 118 as shown in Figure 1B. The implant energy is less than 200 keV, preferably at an energy of approximately 20 to 100 keV, so as not to significantly damage the gate oxide layer 114. Subsequently, the photoresist layer 115 is removed.

Next, the $Si_{1-x}Ge_x$ layer 120 for the channel, as shown in Figure 1C, is grown by solid phase epitaxial (SPE) regrowth, such that lattice mismatch is minimized between the $Si_{1-x}Ge_x$ layer 120 and the underlying Si substrate 110. SPE is performed in a standard silicon processing low temperature furnace, for approximately ten minutes. The furnace temperature is approximately 450 to 700 degrees Celsius, preferably 550 degrees Celsius, to promote SPE regrowth.

A polysilicon gate 122 is then formed on the gate oxide layer 114, as shown in Figure 1C, and source/drain regions 116 are implanted, as well known to one skilled in the art. The resulting structure contains a $Si_{1-x}Ge_x$/Si heterojunction 124 between the channel 120 and the substrate 110. Due to the higher hole mobility in germanium, the field-effect hole mobility is increased significantly, contributing to faster PMOS transistors. Implantation and anneal steps are commonplace in the manufacture of CMOS ICs. Thus, this invention does not add significant cost or complexity to the manufacture of CMOS ICs.

The $Si_{1-x}Ge_x$ channel 120 formed in this invention has a thickness 128, as shown in Figure 1C and the critical values of which are represented by the graph in Figure 2. The critical thickness of the $Si_{1-x}Ge_x$ channel 120 depends on the molar fraction, x, of germanium present in the $Si_{1-x}Ge_x$ layer 120. As long as the critical layer thickness is not exceeded, $Si_{1-x}Ge_x$ 120 will form defect-free during SPE regrowth, as desired. The region 230 below and to the left of the plotted line in Figure 2 is the permissible range of $Si_{1-x}Ge_x$ channel thickness 128 with respect to the molar fraction, x, of germanium. For example, when the molar fraction, x, of germanium is approximately 0.2, as preferred, it is preferable to form a $Si_{1-x}Ge_x$ channel 120, having a thickness 128 of approximately 100 angstroms to 1,000 angstroms, while staying within the critical thickness range.

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.